IDEC Chip Design Contest

A 320 MS/s 2 b/cycle Second order Noise Shaping SAR ADC with Dynamic Amplifier

Ji-Woo Kim and Sang-Gyu Park

Department of Electronic Engineering, Hanyang University

Introduction

- A second-order noise shaping(NS) analog-to-digital (ADC) using a 2bit/cycle successive approximation register (SAR) ADC is proposed.
- With a designated reference digital-to-analog (DAC) and a signal DAC, three comparators in the SAR ADC enable 2-bit conversion in each comparison cycle.
- This chip does not operate well because of the issue in the separating the body of some transistors in FIA.

Proposed Architecture

- ErrorFeedback-NS SAR ADC

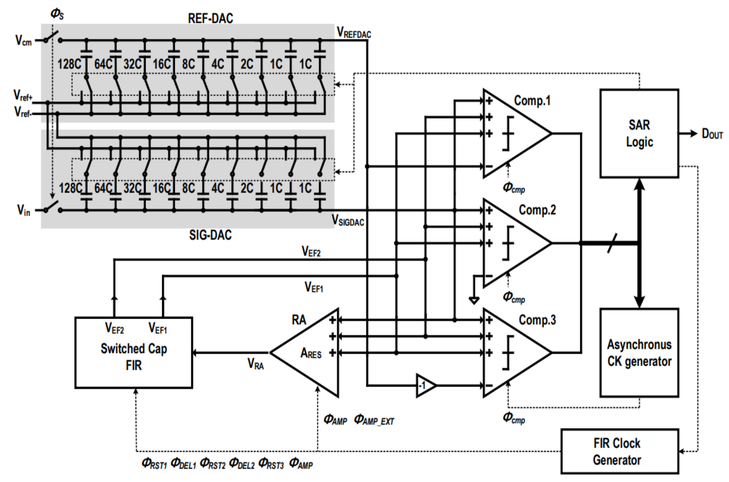

Fig 1. Block diagram of the proposed 2b/cycle NS SAR ADC

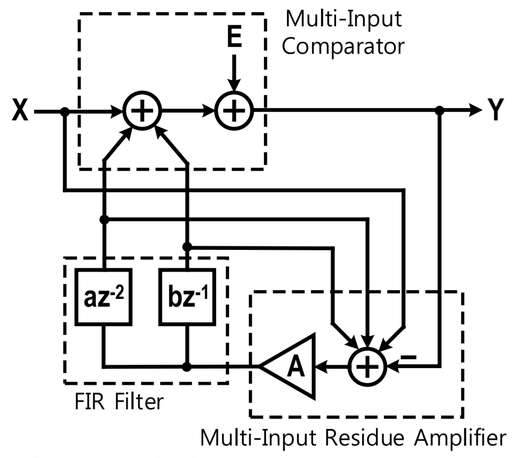

Fig 2. Signal-flow model

- The NTF of the proposed NS SAR ADC could be expressed as

$$NTF(z) = 1 - bz^{-1} + az^{-2} \quad (1)$$

$$b = A_{RES},\ a = bC_1/(C_1 + C_2) \qquad A_{RES} = 1.9\,,\ C_1 = C_2 = 512f$$

- Operation of the 2b/cycle NS SAR ADC

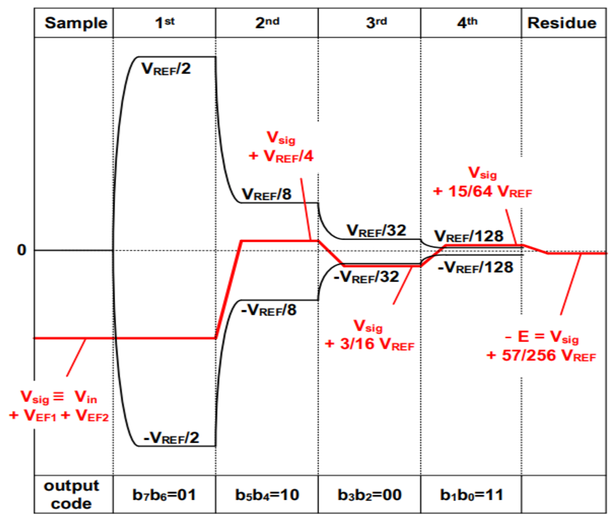

Fig 3. Example of 8-bit 2/b cycle NS SAR operation

- Gain deviation & circuit description

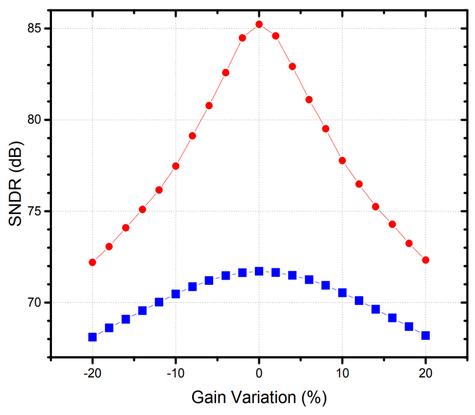

Fig 4.

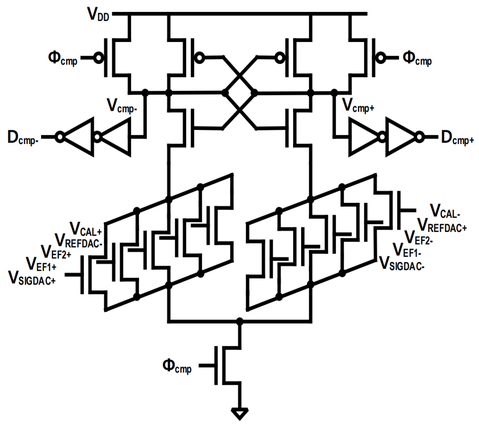

Fig 5.

- Fig 4. Effect of RA gain deviation from the nominal value of 1.9 on SNDR
- Fig 5. Schematic of 5-input Strong-Arm latch comparator

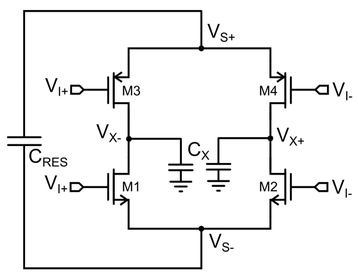

Fig 6.

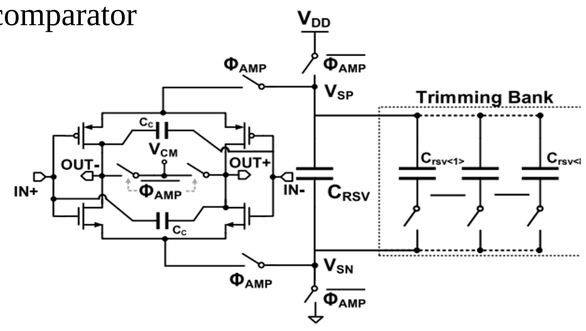

Fig 7.

- Fig 6. Floating Inverter Amplifier(FIA)
- Fig 7. Trimming Bank Circuit

- Effects of Non-idealities

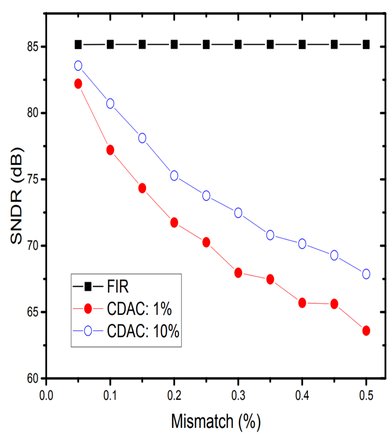

Fig 8.

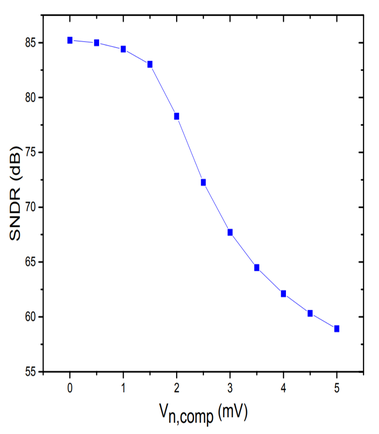

Fig 9.

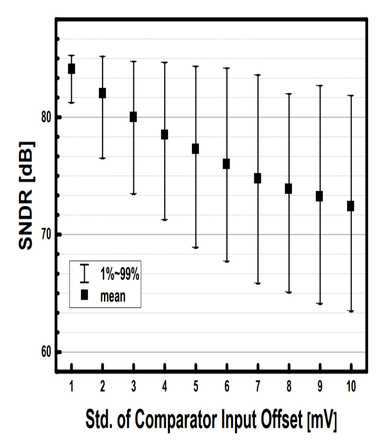

Fig 10.

- Fig 8. Effect of capacitor mismatch on SNDR from behavioral-level Monte-Carlo Simulation (1000 runs for each mismatch)
- Fig 9. SNDR vs Comparator input-referred noise from behavioral-level Monte-Carlo Simulations (1000 runs)
- Fig 10. Comparator offset vs SNDR from behavioral-level Monte-Carlo Simulations

Simulation Results

- Simulation Results

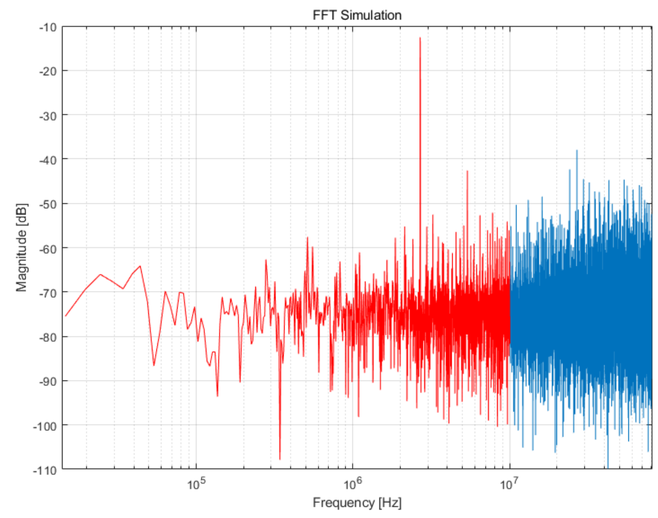

Fig 11. Output spectrum of 2/b cycle NS SAR ADC

- Sampling rate : 320 MS/s
- Supply voltage : 1V
- OSR : 8
- In–band : 10MHz
- NFFT : 4096
- ENOB = 3.7 bits SNDR = 24.37 dB

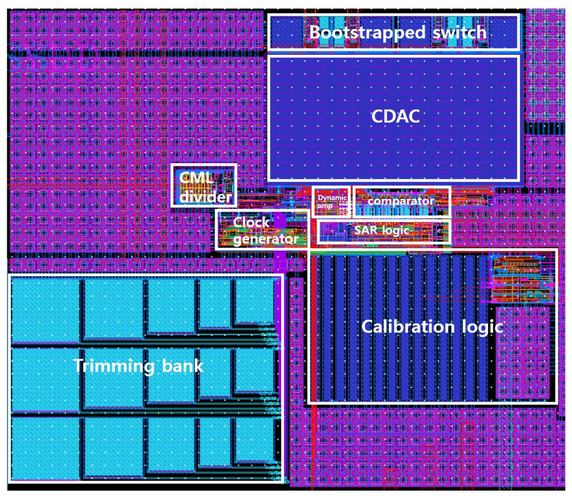

Fig 12. Layout of NS SAR ADC

Fig 13. Chip micrograph of the NS SAR ADC

Conclusion

- By employing 2bit/cycle NS SAR ADC along with EF using FIR filter, a significant improvement in SNDR performance was made possible.
- The gain of RA was lowered and the capacitor of the FIR filter was alternately used to obtain the desired SNDR even for PVT changes.
- Unfortunately, the fabricated chip did not operate as designed due to errors in the separating the body of some transistors in FIA.